# Understanding the Electrical Impact of Edge Contacts in Few-Layer Graphene

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ABSTRACT Two-dimensional layered materials including graphene and transition metal dichalcogenides are identified as promising candidates for various electronic and optoelectronic applications. Due to the weak coupling between individual layers, large contact resistances are frequently found and dominate the performance of layered material systems. In this paper, we employ few-layer graphene as an example to demonstrate a self-aligned edge-contacting scheme for layered material systems. Bypassing the tunneling resistances associated with the weak coupling between layers, lower contact resistances are achieved compared to conventional devices with top contacts. A resistor network model taking into account the gate field screening in the layer stack and all associated resistances is used to quantitatively explain the improvement and compare the current transport in both top-contacted and edge-contacted devices.
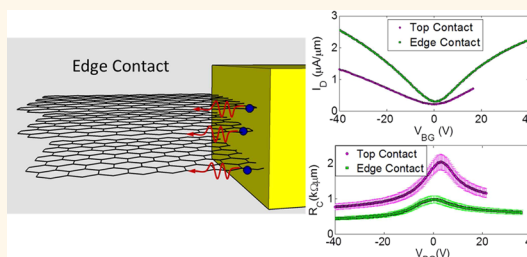
KEYWORDS: few-layer graphene · edge contact · contact resistance · 2D layered materials

Since graphene was experimentally discovered in 2004,[1] it has attracted tremendous interest owing to its outstanding mechanical, thermal, optical, and electrical properties.[2,3] Such properties can lead to revolutions in many applications, including radiofrequency electronics[4,5] and ultrafast photodetectors.[6] Beyond graphene, other 2D materials such as transition metal dichalcogenides (TMDCs) are gaining increasing research interest for their complementary properties that graphene does not offer, for example, a semiconducting band gap.[7] Stacking these 2D building blocks together and creating artificial structures with integrated properties can lead to a new paradigm of "complex materials on demand".[8] While accessing channel materials with low resistive contacts is required for many electronic and optoelectronic applications, making contacts to multiple-layer structures bonded by weak van de Waals forces has not yet been carefully studied. In the following context, we will use few-layer graphene (FLG) as an example to demonstrate the advantage of using edge contacts over conventional top contacts. The same contact scheme can be easily adopted for other 2D layered materials.

For all high-mobility channel materials like graphene, low contact resistances are crucial to achieve high device performance.

Conventional source/drain (S/D) contacts are usually formed by depositing metal electrodes onto the graphene surface. Optimization of the contact resistance in single-layer graphene (SLG) field-effect transistors (FETs) has mainly focused on selecting metals with proper work functions and improving the graphene-to-metal interface. The lowest contact resistance reported to date is ~200 $\Omega \mu$m at carrier concentrations of 10^{13}/cm^2, using palladium (Pd) contacts.[9,10]

In the FLG case, although more conduction channels are available, the device on-state current decreases with the graphene layer number, as shown in Figure 1b. Similar observations were reported by others,[11,12] and a resistor network model considering the coupling between graphene layers and gate field screening effect had been proposed.[12] It was suggested that in back-gated multilayer graphene devices, a rather small Thomas−Fermi screening length of $\lambda = 0.6$ nm in the on-state confines most charges induced by the back gate to be mirrored in the graphene layers closest to the substrate surface.[13] While this conclusion is reasonable for semiconducting materials that need a finite gate field to reach the device on-state, being a zero band gap material, graphene layers on the top of the stack are able to carry non-negligible
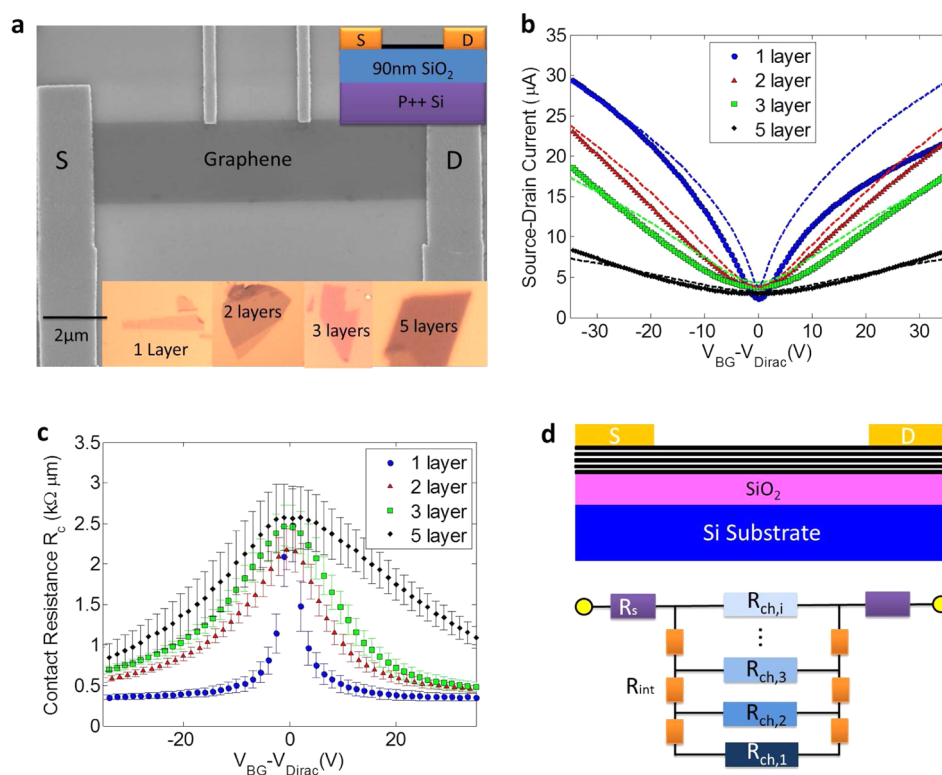
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Figure 1. (a) SEM image of a four-terminal FLG device. Bottom inset shows optical images of graphene flakes with various thicknesses; top inset is the device cross-section schematic. (b) Transfer characteristics of conventional top-contacted FLG FETs with graphene layer numbers of 1, 2, 3, and 5. Source−drain currents of all devices are normalized by the respective channel length and width for direct comparison. Dashed lines are fits from the resistor network model illustrated in part (d). (c) Contact resistance, R_C, as a function of the gate voltage. Error bars account for the finite widths of the voltage leads. (d) Resistor network model for conventional top-contacted FLG devices.

currents despite the small gate screening length. Moreover, we find the resistance associated with the tunneling between graphene layers under the S/D contacts to be rather large taking into account that current is injected only within the contact transfer length. The resistance network model is therefore modified here to reflect these two changes.

To maximize the on-state performance and access the high-mobility channels more directly, it is important to eliminate the tunneling resistances mentioned above. In this paper, a novel contact scheme for FLG FETs is explored in detail. Using a self-aligned process, graphene is etched and carbon atoms at the cut edges are directly contacted by a subsequently deposited metal layer. The covalent/ionic bonds formed between metal and carbon atoms allow for a lower contact resistivity compared to the weak van de Waals bonds under conventional top contacts.[14] More importantly, these edge contacts bypass the tunneling resistances between layers and allow direct current injection into individual graphene layers. An about 2 times lower contact resistance is observed in edge-contacted FLG devices compared to those with conventional top contacts. Finally, by comparing devices with different numbers of graphene layers, bilayer graphene FETs with edge contacts are identified to exhibit the best device performance. FLG FETs with more graphene

layers do not reach higher on-state current levels due to effective gate field screening, which also leads to lower current modulation ratios.

RESULTS AND DISCUSSIONS

A scanning electron microscope (SEM) image of a four terminal, top-contacted graphene field effect device is shown in Figure 1a. Details of the device fabrication process are described in the Methods section. Graphene flakes with different layer thicknesses were identified by their optical reflection contrast (Figure 1a inset), as well as Raman spectroscopy and atomic force microscope (AFM) images. Transfer characteristics of four top-contacted FLG devices with various graphene layer thicknesses are shown in Figure 1b. As mentioned above, thicker graphene devices show substantially lower on-state currents. The contact resistance as a function of the gate voltage extracted from four-terminal measurements is presented in Figure 1c for all devices. A clear trend of increasing contact resistance with graphene layer number is observed.

A resistor network model proposed by Sui et al.[12] is adopted here to understand the transport characteristics in detail, as shown in Figure 1d. When current is injected into the FLG channel, charges are transmitted through the contact interfaces and tunnel into the

graphene layers that are not in direct contact with the S/D metals. Three resistances are included in the model: the contact interface resistance, R_s; the interlayer tunneling resistance, R_{int}; and the channel resistance of the ith graphene layer, $R_{ch,i}$. R_s exists in SLG devices as well and is measured to be $R_s = 200\ \Omega\mu$m. $R_{int} = \rho_c d_{ML}/A$, where $\rho_c = 0.3\ \Omega$m is the tunneling resistivity, $d_{ML} = 0.3$ nm is the distance between two graphene layers, and A is the area under S/D contacts within the contact transfer length in which current is injected. Since the contact transfer length L_T ranges from 50 to 250 nm, R_{int} is thus determined for every device, and its value ranges from 410 to 2100 Ω. To understand the impact of R_{int}, let us compare the resistor network model with and without R_{int}. Without considering R_{int}, all graphene layers in the stack are connected to S/D contacts directly, and the total resistance of the network can be calculated by $R_{tot} = 2R_s + 1/\sum_{i=1}^{N}(1/R_{ch,i})$. Taking into account R_{int}, $2(N-i)R_{int}$ is added to the ith graphene layer and the total resistance of the network becomes $R'_{tot} = 2R_s + (1/\sum_{i=1}^{N}1/(R_{ch,i} + 2(N-i)R_{int}))$. Consequently, the effective value of all R_{int} counted in the network can be calculated by $R_{int,eff} = R'_{tot} - R_{tot} = (1/[\sum_{i=1}^{N}1/(R_{ch,i} + 2(N-i)R_{int})]) - 1/(\sum_{i=1}^{N}(1/R_{ch,i}))$, which can be viewed as an additional contact resistance. Different from SLG FETs, in which the contact resistance is dominated by R_s, FLG FETs have larger contact resistances due to the contribution from $R_{int,eff}$. Owing to the gate field screening from the bottom graphene layers, charges are not equally distributed among all layers. A simple Thomas–Fermi screening model is used to calculate the charge distribution.[12] Considering diffusive transport in our long-channel devices, the channel resistance $R_{ch,i} = L/(Wn_iq\mu)$ can be calculated, where L and W are the channel length and width, respectively, μ is the effective mobility, and n_i is the charge in each layer. Due to the short gate field screening length in FLG of $\lambda \approx 0.6$ nm, top graphene layers do not get "turned on" by the back gate efficiently and appear to have larger channel resistances compared to the bottom layers. Transfer characteristics simulated from the resistor network model in Figure 1d show good agreement with the experimental measurements, as shown in Figure 1b.

Since R_{int} is rather large and prevents current from reaching the less resistive graphene layers at the bottom, eliminating R_{int} is expected to improve the on-state performance of FLG devices. It has been shown that edge contacts to open carbon bonds in carbon nanotubes or graphene substantially reduce contact resistances compared to top contacts.[14−17] However, experimentally realizing a true edge contact to FLG is nontrivial. Since current injection over a length scale beyond the transfer length is negligible, etching graphene to expose edges for contact formation requires the distance between the graphene edge

and the metal contact edge to be smaller than the transfer length, as illustrated in Figure 2a. However, the finite lithographical alignment accuracy does not allow for a reliable edge contact formation in this manner.

To accurately position metal contacts at graphene edges within the transfer length, a self-aligned fabrication process is developed here. For direct comparison, the same graphene devices with conventional top contacts shown in Figure 1 are used to fabricate edge contacts. Detailed edge contact fabrication steps are described in the Methods section. In brief, after three continuous steps of contact patterning, graphene etching, and resist overdeveloping, graphene edges were exposed and directly contacted by subsequently deposited metal electrodes, and the actual metal/graphene contact lengths can be precisely controlled by the overdevelopment time, as shown in Figure 2b. The inset shows an SEM picture of a graphene flake covered by poly(methyl methacrylate) (PMMA), etched in the open PMMA window, and a small stripe uncovered after the extra resist development. As highlighted at the edge of the PMMA window, ~100 nm long graphene with fresh edges is exposed for contact formation in this case. The final S/D contact structure consists of an edge contact in connection with a 100 nm long top contact.

Two representative edge-contacted devices with five- and two-layer graphene are presented in Figure 2c and d, respectively, in comparison with the original devices using conventional top contacts. Significant on-state current improvements are observed in edge-contacted devices for both layer thicknesses. Note that the device channel lengths are sufficiently long so that the small length reduction due to etching will not impact the on-state current. Contact resistances of these devices are extracted from four-terminal measurements and presented in Figure 2e and f. Compared to conventional top contacts, contact resistances are lowered approximately by a factor of 2 in edge-contacted graphene devices.

To understand the observed improvement, a modified resistor network model is utilized for edge-contacted graphene devices, as shown in Figure 2a. In addition to the existing resistances from the conventional resistance network, R_{edge} is added to account for the resistance between the metal contact and graphene edge at each layer. $R_{edge} = 150−360\ \Omega\mu$m is extracted from curve fitting using the edge contact model. While for an N-layer FLG FET with top contacts, current injection to the bottom graphene layer needs to go through $2(N-1)$ tunneling resistances, our novel self-aligned edge contact scheme allows current to be directly injected to each graphene layer, bypassing large tunneling resistances by the relatively small R_{edge}.

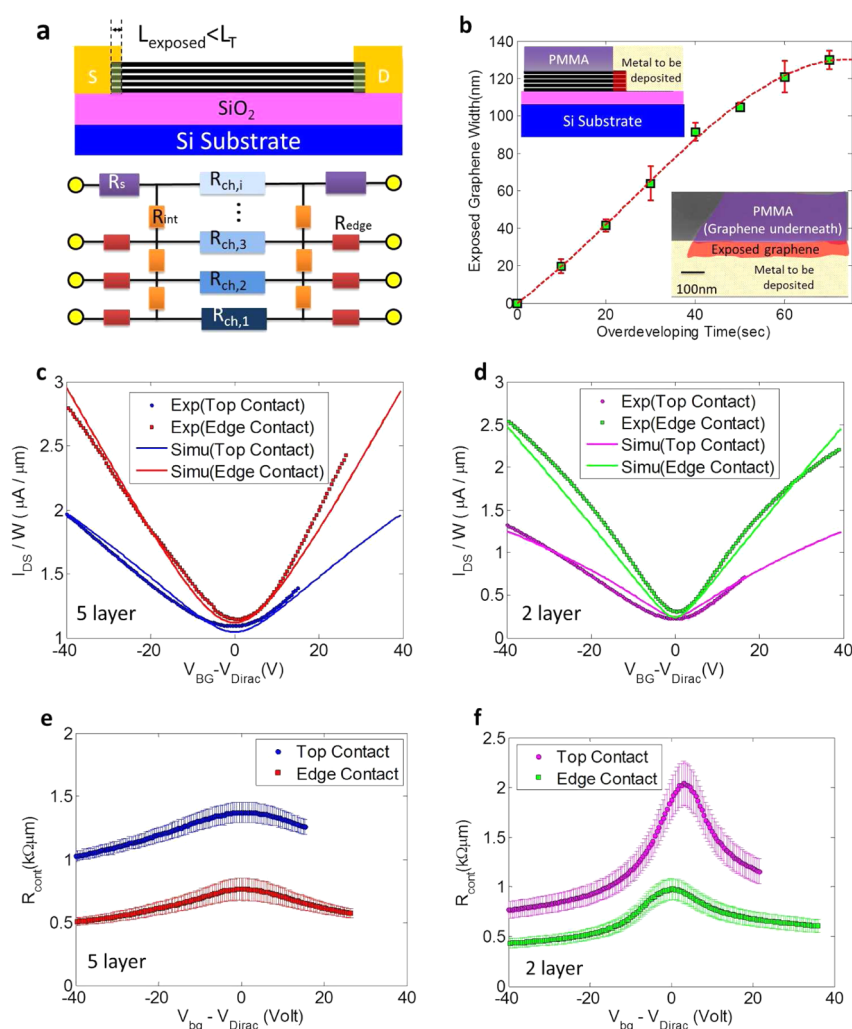Next we have calculated the current distribution in FLG devices for the two contacting schemes using the

Figure 2. (a) Resistor network model of edge-contacted FLG FETs. **(b)** Exposed graphene contact length *vs* overdeveloping time. Bottom inset is the top-view SEM image of a graphene flake covered by PMMA with an exposed region, obtained after 50 s developing, O_2 RIE, and 40 s overdevelopment. Top inset is the cross-section sketch of the SEM picture. **(c)** Transfer characteristics of a top-contacted (blue dots) and edge-contacted (red dots) five-layer graphene FET. The blue and red solid lines are simulated curves from the resistor network model. **(d)** Transfer characteristics of a top-contacted (purple dots) and edge-contacted (green dots) bilayer graphene FET. The purple and green solid lines are simulated curves. **(e)** Contact resistance comparison of a five-layer graphene FET with top contacts (blue) and edge contacts (red). **(f)** Contact resistance comparison of a bilayer graphene FET with top contacts (purple) and edge contacts (green).

corresponding resistor network model. In Figure 3a, current in each graphene layer of a bilayer FET with conventional top contacts is simulated. The bottom layer close to the gate is labeled as the first layer. In the Dirac point regime, the off-state current in the first layer is smaller than that in the second layer because of the existing tunneling resistance. On the other hand, at the device on-state, current of the second layer becomes lower due to efficient gate field screening, despite the existing tunneling resistance. In contrast, the edge-contacted bilayer graphene device shows a drastically different current distribution, as shown in Figure 3b. Since weak screening occurs in the Dirac point regime and the edge contact resistance to the first graphene layer is comparable to the interface resistance to the second layer, similar currents are found in each graphene layer. At the device on-state,

the first graphene layer can now carry much higher current than the second layer due to the efficient gate field control and direct contacts through the edges. Compared to the top-contacted device, this graphene layer in an edge-contacted device now carries more than 3 times the current. Similar current distribution simulations are performed for a five-layer graphene FET with both the top and edge contacts, as shown in Figure 3c and d. In the five-layer stack, due to the relatively small on-state screening length of $\lambda \approx 0.6$ nm mentioned above, the top three layers far from the back gate contribute much less current compared to the bottom two layers, especially in the edge-contacted case.

Transfer characteristics of the edge-contacted bilayer and five-layer graphene FET are compared in Figure 4a. The five-layer device provides higher currents in both device on- and off-states. However, one of
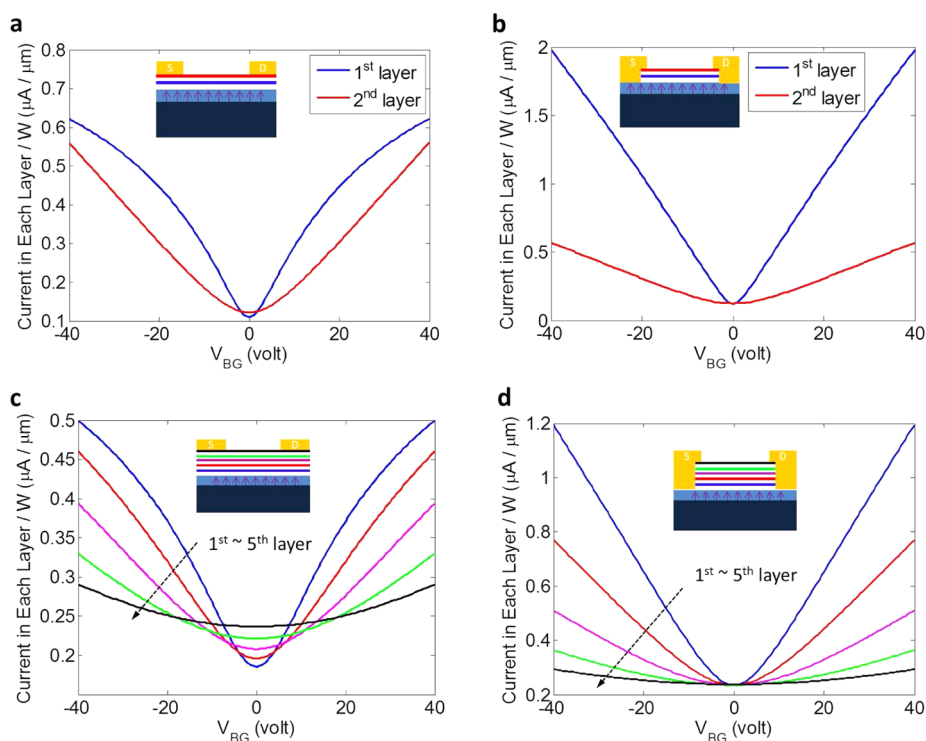
Figure 3. Current distribution in each graphene layer of (a) conventional top-contacted bilayer graphene FET, (b) edge-contacted bilayer graphene FET, (c) conventional top-contacted five-layer graphene FET, (d) edge-contacted five-layer graphene FET, based on the new resistor network model using the following parameters: λ = 0.6 nm, d_{ML} = 0.3 nm, R_s = 200 $\Omega\mu$m, R_{int} = 1600 Ω, R_{edge} = 320 $\Omega\mu$m, μ = 1600 cm^2/V·s, z = 2 for the bilayer and z = 4 for the five-layer graphene device. z is the minimal conductance factor.
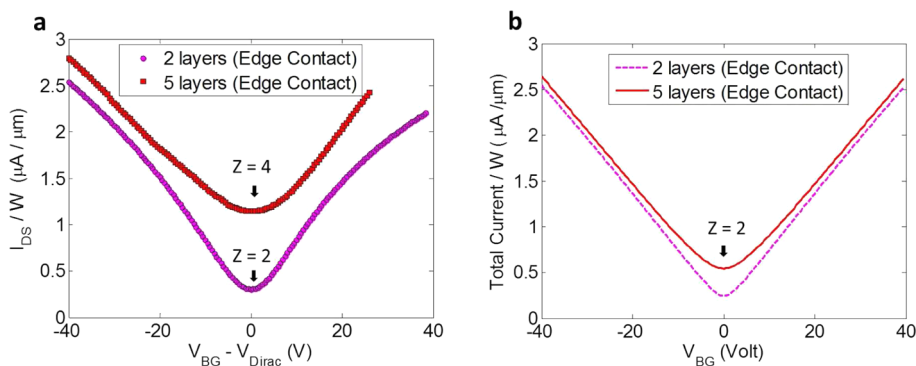

Figure 4. (a) Transfer characteristics of an edge-contacted bilayer graphene FET (purple dots) and an edge-contacted five-layer device (red dots). Note that the minimal conductance factor z is different for the bilayer and the five-layer graphene device. (b) Comparison of characteristics of an edge-contacted bilayer (purple dash) and five-layer graphene FET (red solid) assuming z = 2 for both cases. Both currents are normalized by channel width, and the channel lengths are ~10 μm.

the complexities in graphene devices is that the minimum conductance is largely impacted by the trap charge condition of the underlying SiO$_2$ substrate.[18,19] If this external substrate effect is set to be the same for both devices artificially (by setting z to be the same, =2), the five-layer device does not carry much larger current than the bilayer device, shown in Figure 4b. Due to the small screening length in FLG, most of the current flows in the first few graphene layers close to the back gate. With direct access to the bottom layers through edge contacts, adding more graphene layers

far from the gate does not further improve the device performance.

SUMMARY AND CONCLUSIONS

In conclusion, we have demonstrated a novel edge contact scheme for FLG devices and achieved a 2× current improvement in the device on-state. Two resistor network models are used to extract relevant contact resistance information for both top-contacted and edge-contacted FLG devices and to compare the current distribution in the two. The same edge contact

fabrication and modeling schemes can be applied to other 2D layered material stacks with proper modifications to the gate field screening length and individual contact resistance values.

METHODS

Single-layer and few-layer graphene devices under study were prepared from mechanically exfoliated graphene on top of a 90 nm SiO_2/p++ Si substrate. The graphene layer thickness was identified by optical reflection contrast, as shown in the bottom inset of Figure 1a.[20] AFM and Raman spectroscopy were also used to verify the thicknesses. Graphene channels were patterned by e-beam lithography, followed by O_2 RIE etching. Four-terminal electrodes were defined by another e-beam lithography step, and a 1 nmTi/20 nmPd/10 nmAu stack was deposited. Figure 1a shows an SEM image of a final device.

After electrical measurements of the top-contacted devices, edge contacts were patterned on the same graphene flakes for direct comparison. An e-beam lithography step defined open PMMA windows close to the original S/D top contacts. Graphene in these windows got etched away by O_2 RIE, and fresh edges were exposed. An extra PMMA development step was added to uncover some graphene areas for additional contact coverage. In this way, the actual metal/graphene contact lengths can be precisely controlled by the development time, as shown in Figure 2b. All measurements were performed in a probe station after an overnight vacuum annealing at 400 K.

Conflict of Interest: The authors declare no competing financial interest.

REFERENCES AND NOTES

1. Novoselov, K. S.; Geim, A. K.; Morozov, S. V; Jiang, D.; Zhang, Y.; Dubonos, S. V; Grigorieva, I. V.; Firsov, A. A. Electric Field Effect in Atomically Thin Carbon Films. *Science* **2004**, *306*, 666–669.
2. Novoselov, K. S.; Fal'ko, V. I.; Colombo, L.; Gellert, P. R.; Schwab, M. G.; Kim, K. A Roadmap for Graphene. *Nature* **2012**, *490*, 192–200.
3. Bonaccorso, F.; Sun, Z.; Hasan, T.; Ferrari, A. C. Graphene Photonics and Optoelectronics. *Nat. Photonics* **2010**, *4*, 611–622.
4. Wu, Y.; Lin, Y.; Bol, A. A.; Jenkins, K. A.; Xia, F.; Farmer, D. B.; Zhu, Y.; Avouris, P. High-Frequency, Scaled Graphene Transistors on Diamond-Like Carbon. *Nature* **2011**, *472*, 74–78.
5. Han, S.-J.; Garcia, A. V.; Oida, S.; Jenkins, K. A.; Haensch, W. Graphene Radio Frequency Receiver Integrated Circuit. *Nat. Commun.* **2014**, *5*, 1–6.
6. Xia, F.; Mueller, T.; Lin, Y.-M.; Valdes-Garcia, A.; Avouris, P. Ultrafast Graphene Photodetector. *Nat. Nanotechnol.* **2009**, *4*, 839–843.
7. Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-Layer MoS_2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147–150.
8. Novoselov, K. S.; Castro Neto, A. H. Two-Dimensional Crystals-Based Heterostructures: Materials with Tailored Properties. *Phys. Scr.* **2012**, *T146*, 014006.
9. Xia, F.; Perebeinos, V.; Lin, Y.; Wu, Y.; Avouris, P. The Origins and Limits of Metal−Graphene Junction Resistance. *Nat. Nanotechnol.* **2011**, *6*, 179–184.
10. Knoch, J.; Chen, Z.; Appenzeller, J. Properties of Metal-Graphene Contacts. *IEEE Trans. Nanotechnol.* **2012**, *11*, 513–519.
11. Nagashio, K.; Nishimura, T.; Kita, K.; Toriumi, A. Systematic Investigation of the Intrinsic Channel Properties and Contact Resistance of Monolayer and Multilayer Graphene FET. *Jpn. J. Appl. Phys.* **2010**, *49*, 051304.
12. Sui, Y.; Appenzeller, J. Screening and Interlayer Coupling in Multilayer Graphene Field-Effect Transistors. *Nano Lett.* **2009**, *9*, 2973–2977.
13. Das, S.; Appenzeller, J. Where Does the Current Flow in Two-Dimensional Layered Systems? *Nano Lett.* **2013**, *13*, 3396–3402.
14. Matsuda, Y.; Deng, W.; Goddard, W. A., III. Contact Resistance for "End-Contacted" Metal - Graphene and Metal - Nanotube Interfaces from Quantum Mechanics. *J. Phys. Chem. C* **2010**, *114*, 17845–17850.
15. Wang, L.; Meric, I.; Huang, P. Y.; Gao, Q.; Gao, Y.; Tran, H.; Taniguchi, T.; Watanabe, K.; Campos, L. M.; Muller, D. A; *et al*. One-Dimensional Electrical Contact to a Two-Dimensional Material. *Science* **2013**, *342*, 614–617.
16. Khatami, Y.; Li, H.; Xu, C. Metal-to-Multilayer-Graphene Contact—Part I: Contact Resistance Modeling. *IEEE Trans. Electron Dev.* **2012**, *59*, 2444−2452.
17. Chu, T.; Chen, Z. Graphene Nanomesh Contacts and Its Transport Properties. *Device Res. Conf.* **2012**, 185–186.
18. Martin, J.; Akerman, N.; Ulbricht, G.; Lohmann, T.; Smet, J. H.; von Klitzing, K.; Yacoby, A. Observation of Electron−Hole Puddles in Graphene Using a Scanning Single-Electron Transistor. *Nat. Phys.* **2007**, *4*, 144–148.
19. Chen, J.-H.; Jang, C.; Xiao, S.; Ishigami, M.; Fuhrer, M. S. Intrinsic and Extrinsic Performance Limits of Graphene Devices on SiO_2. *Nat. Nanotechnol.* **2008**, *3*, 206–209.
20. Blake, P.; Hill, E. W.; Castro Neto, A. H.; Novoselov, K. S.; Jiang, D.; Yang, R.; Booth, T. J.; Geim, A. K. Making Graphene Visible. *Appl. Phys. Lett.* **2007**, *91*, 063124.